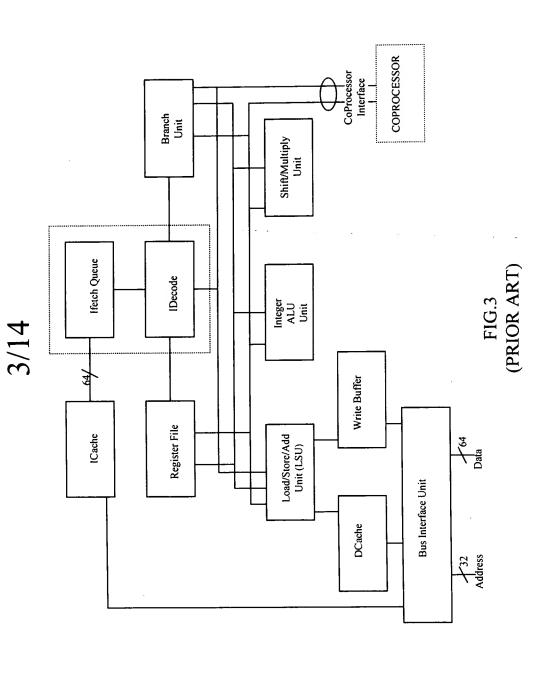
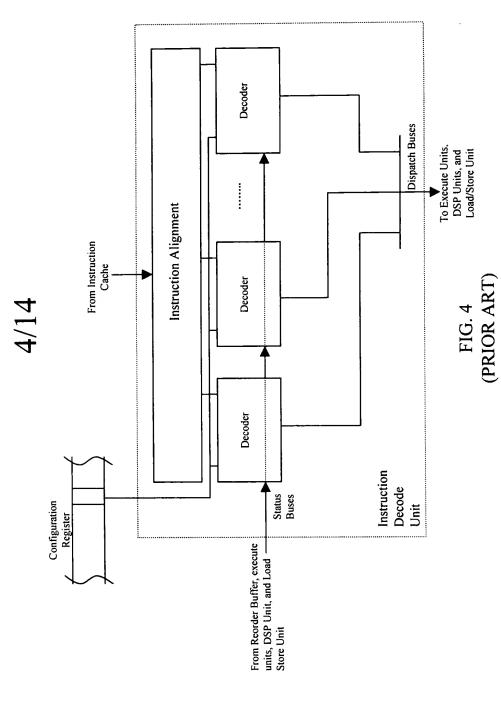


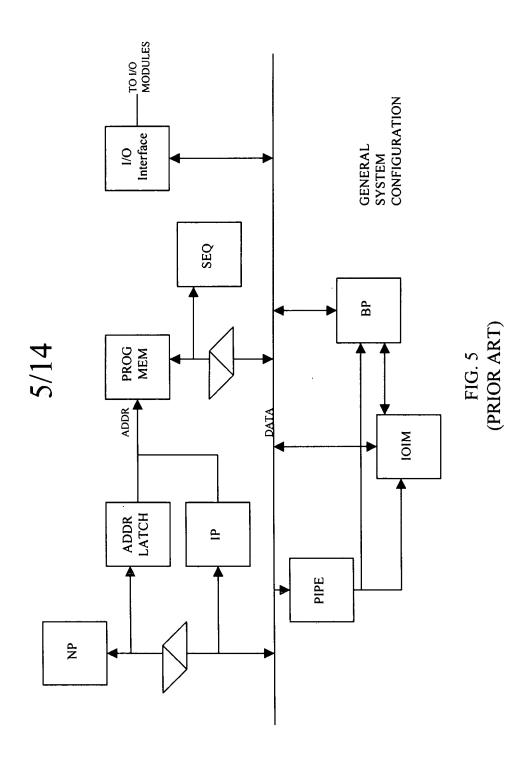
FIG. 1 (PRIOR ART)

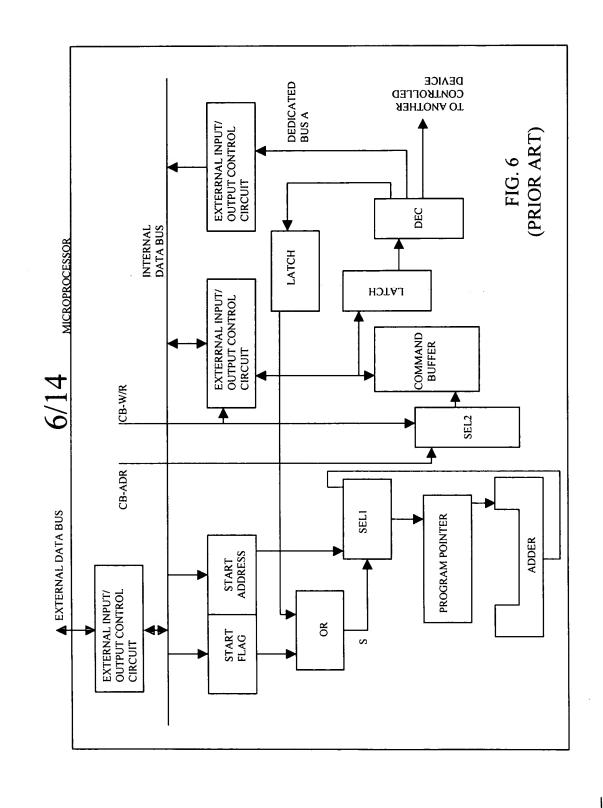
Coprocessor	Compatible Processor	Coprocessor Characteristics
Intel 8087	Intel 8086/8088	5 Mhz, 70 cycles for add & 700 cycles for log
Intel 80287	Intel 80286	12.5 Mhz, 30 cycles for add & 264 cycles for log
Intel 387DX	Intel 386DX	33 Mhz, 12 cycles for add & 210 cycles for log
Intel i486	Intel i486 (same chip)	33 Mhz, 8 cycles for add & 171 cycles for log
Motorola MC68882	Motorola MC68020/68030	40 Mhz, 56 cycles for add & 574 cycles for log
Weitek 3167	Intel 386DX	33 Mhz, 6 cycles for add & 365 cycles for log by software emulation
Weitek 4167	Intel i486	33 Mhz, 2 cycles for add & not available for log

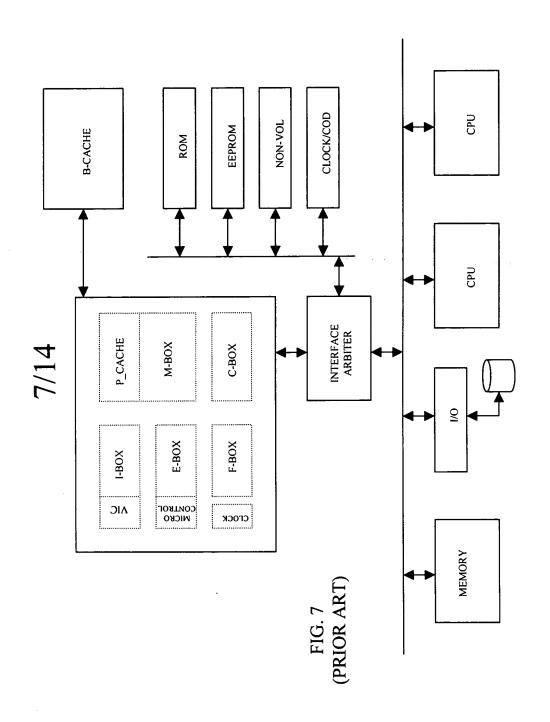
FIG. 2 (PRIOR ART)

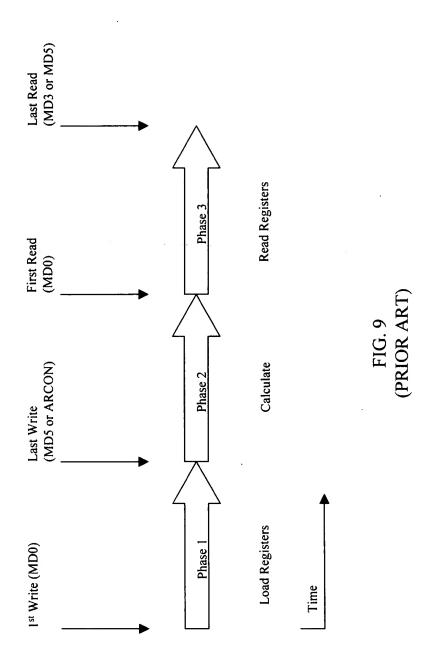












Operation	Result	Remainder	Execution Time
32-bit/16-bit	32-bit	16-bit	6 tcy
16-bit/16-bit	16-bit	16-bit	4 tcy
16-bit x 16-bit	32-bit	-	4 tcy
32-bit normalize	1	-	6 tcy
32-bit shift left/right	1	•	6 tcy

## Notes:

- 1) 1 tcy = 1 microsecond at 12 Mhz Oscillator frequency
- 2) The maximum shift speed is 6 shifts per machine cycle

FIG. 10 (PRIOR ART)

	0.0			00000b,
-	S		t Left	izing is ner than
	SC.1		ht or Shif	CNT1, CNT0 000b, normal rith values oth
2	SC.2	**	SLR = Shift Right or Shift Left 1 = Shift Right 0 = Shift Left	CNT4,CNT3,CNT2,CNT1,CNT0 Shift Counter When preset with 00000b, normalizing is Selected. When set with values other than 00000b, Shift operation is selected.
3	SC.3		<b>SLR</b> : 1 = SI 0 = SI	CNT4, Shift C When I Selecte Shift o
4	SC.4 SC.3 SC.2 SC.1 SC.0		peu	æ
5			erly perform by hardware	riggered by previous pleted.
9	MDEF MDOV SLR		MDEF = Error flag  1 = Indicates an improperly performed operation. MDEF is set by hardware	when an operation is retriggered by a write access before the previous operation has been completed.  0 = Reset value.
7	MDEF		MDEF = Error flag  1 = Indicates an improperation. MDEF is s	when an operati write access bef operation has be 0 = Reset value.

FIG. 11 (PRIOR ART)

MDEF = Overflow flag

Exclusively controlled by hardware. MDOV is set by following events:
-division by zero
- multiplication with result greater than 0FFFFh

0 = Reset value.

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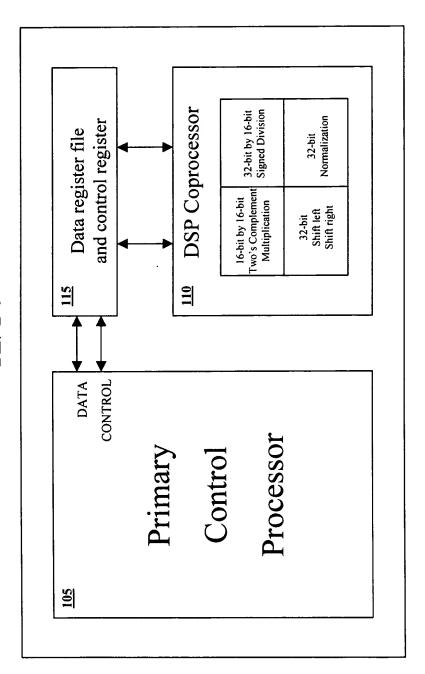
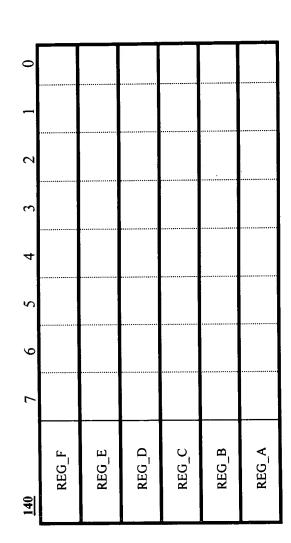


FIG. 12

	-				
0	CNT0		Left	ation	
-	MO SLSR CNT4 CNT3 CNT2 CNT1 CNT0		SLSR = Shift Right or Shift Left 1 = Shift Right 0 = Shift Left	CNT4,CNT3,CNT2,CNT1,CNT0 Shift Count for SLSR or Normalization Input for SLSR Output for Normalization	
2	CNT2		SLSR = Shift R 1 = Shift Right 0 = Shift Left	CNT4, CNT3, CNT2, CNT1, CNT0 Shift Count for SLSR or Normaliz Input for SLSR Output for Normalization	
3	CNT3	130	= 0 = 1 STS	CN1 Shift Inpu	135
4	CNT4	'			
5	SLSR		uc	oit divide oit multiply peration lization	
9	МО		Operation	0 32-bit by 16-bit divide 1 16-bit by 16-bit multiply 0 32-bit Shift operation 1 32-bit Normalization	
120 7	M1	125	M1 M0	0 - 0 - 0	

FIG. 13



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QUOTIENT = (REG\_F,REG\_E,REG\_D,REG\_C)

(REG\_B,REG\_A)

QUOTIENT = (REG\_F,REG\_E,REG\_D,REG\_C)

REMAINDER = (REG\_B, REG\_A)

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MULTIPLICATION = (REG\_D,REG\_C) X (REG\_B,REG\_A)
PRODUCT = (REG\_D,REG\_C,REG\_B,REG\_A)
REG\_F, and REG\_E are unused

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SHIFT LEFT, SHIFT RIGHT & NORMALIZATION (REG\_D,REG\_C,REG\_B,REG\_A)
REG\_F, and REG\_E are unused

FIG. 14